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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	TOD PAULUS ET AL.
Filed:	February 12, 2002
For:	DC OFFSET REDUCTION IN RADIO-FREQUENCY APPARATUS AND ASSOCIATED METHODS
Serial No.:	10/074,676
Group Art Unit:	UNKNOWN
Examiner:	UNKNOWN
Atty Docket No.:	SILA:098

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on the date below:

5-9-02 Marty Bowen
Date Name

Assistant Commissioner For Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Please amend the application as follows.

In the specification:

The rewritten clean versions of all the specification changes are provided below. Attached at the end of this paper is an Appendix providing an indication of the changes relative to the prior version of the specification, as now required by Rule 121.

Please replace the paragraph beginning on page 1, line 27 and ending on page 2, line 2 with the following:

Furthermore, this patent application incorporates by reference the following patent documents: U.S. Patent Application Serial No. 10/075,122, Attorney Docket No. SILA:078, titled "Digital Architecture for Radio-Frequency Apparatus and Associated Methods"; and U.S. Patent Application Serial No. 10/075,099, Attorney Docket No.

05/30/2002 ZJUHAR1 00000029 10074676
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SILA:097, titled "Notch Filter for DC Offset Reduction in Radio-Frequency Apparatus and Associated Methods."

In the Claims:

Please cancel claim 2 and add new claims 3-44.

The rewritten clean versions of all the pending claims are provided below. Attached at the end of this paper is an Appendix providing an indication of the changes relative to the prior version of the claims, as now required by Rule 121(c).

1. A radio-frequency (RF) receiver circuitry, comprising:

down-converter circuitry configured to accept a received radio-frequency signal, the down-converter circuitry further configured to process the received radio-frequency signal to provide an in-phase down-converted signal and a quadrature down-converted signal;

analog-to-digital converter (ADC) circuitry configured to receive the in-phase and quadrature down-converted signals and to provide an in-phase digital output signal and a quadrature digital output signal; and

DC offset reduction circuitry coupled to the analog-to-digital converter circuitry,

wherein the DC offset reduction circuitry tends to reduce a DC offset transmitted to the in-phase and quadrature digital output signals.

3. The radio-frequency receiver circuitry of claim 1, further comprising:

a combiner circuitry configured to provide to the analog-to-digital circuitry an in-phase difference signal and a quadrature difference signal,

wherein the combiner circuitry subtracts an in-phase output signal of the DC offset reduction circuitry from the in-phase down-converted signal to produce the in-phase difference signal, and

wherein the combiner circuitry subtracts a quadrature output signal of the DC offset reduction circuitry from the quadrature down-converted signal to produce the quadrature difference signal.

4. The radio-frequency receiver circuitry of claim 3, wherein the DC offset reduction circuitry further comprises a digital-to-analog circuitry configured to provide the in-phase and quadrature output signals of the DC offset reduction circuitry.

5. The radio-frequency receiver circuitry of claim 4, wherein the DC offset reduction circuitry further comprises a filter circuitry configured to process the in-phase and quadrature digital output signals to provide an in-phase filtered digital output signal and a quadrature filtered digital output signal, the filter circuitry further configured to provide the in-phase and quadrature filtered digital output signals to the digital-to-analog circuitry.

6. The radio-frequency receiver circuitry of claim 5, wherein a transfer function of the DC offset reduction circuitry has at least one pole the location of which is adjustable over an adjustment cycle of the DC offset reduction circuitry.

7. The radio-frequency receiver circuitry of claim 6, wherein the location of the at least one pole is adjusted in an initial part of the adjustment cycle of the DC offset reduction circuitry so that the DC offset reduction circuitry tends to settle quickly.

8. The radio-frequency receiver circuitry of claim 7, wherein the location of the at least one pole is further adjusted in a later part of the adjustment cycle of the DC offset reduction circuitry so that the DC offset reduction circuitry tends to remove the DC offset more accurately.

[redacted]

9. The radio-frequency receiver circuitry of claim 8, wherein the location of the at least one pole is adjusted by modifying a gain of the DC offset reduction circuitry.

10. The radio-frequency receiver circuitry of claim 9, wherein the location of the at least one pole is adjusted before a reception of a burst of data begins.

11. The radio-frequency receiver circuitry of claim 10, wherein the in-phase and quadrature output signals of the DC offset reduction circuitry become substantially constant before the reception of the burst of data begins.

12. The radio-frequency receiver circuitry of claim 11, wherein the filter circuitry comprises a digital filter circuitry.

13. The radio-frequency receiver circuitry of claim 12, wherein the digital filter circuitry comprises a low-pass filter circuitry.

14. The radio-frequency receiver circuitry of claim 13, wherein the low-pass filter circuitry comprises an integrator circuitry.

15. The radio-frequency receiver circuitry of claim 14, wherein the analog-to-digital converter circuitry comprises a sigma-delta analog-to-digital converter circuitry.

16. The radio-frequency receiver circuitry of claim 15 used in a radio-frequency transceiver circuitry.

17. The radio-frequency receiver circuitry of claim 15 used in a low intermediate-frequency (IF) radio-frequency receiver circuitry.

18. A radio-frequency (RF) receiver circuitry, comprising:

receiver analog circuitry included within a first integrated circuit, the receiver analog circuitry, comprising:

down-converter circuitry configured to receive and down-convert a radio-frequency input signal to generate a down-converted signal;

an analog-to-digital converter circuitry to convert the down-converted signal to a digital output signal; and

DC offset reduction circuitry coupled to the analog-to-digital converter circuitry, wherein the DC offset reduction circuitry tends to reduce a DC offset of the receiver analog circuitry; and

receiver digital circuitry included within a second integrated circuit, the receiver digital circuitry configured to receive and process the digital output signal to generate a processed digital signal.

19. The radio-frequency receiver circuitry of claim 18, further comprising a combiner circuitry configured to provide a difference signal to the analog-to-digital circuitry, wherein the combiner circuitry subtracts an output signal of the DC offset reduction circuitry from the down-converted signal to produce the difference signal.

20. The radio-frequency receiver circuitry of claim 19, wherein the DC offset reduction circuitry further comprises a feedback loop that includes a cascade coupling of a filter circuitry and a digital-to-analog circuitry, wherein the filter circuitry receives the digital output signal, and wherein the digital-to-analog circuitry provides the output signal of the DC offset reduction circuitry.

21. The radio-frequency receiver circuitry of claim 20, wherein a transfer function of the DC offset reduction circuitry has at least one pole the location of which is adjustable so as to modify the settling time of the DC offset reduction circuitry.

22. The radio-frequency receiver circuitry of claim 21, wherein the location of the at least one pole is adjusted at an initial point in time so that the DC offset reduction circuitry tends to settle quickly.

23. The radio-frequency receiver circuitry of claim 22, wherein the location of the at least one pole is adjusted at least once more after the initial point in time so that the DC offset reduction circuitry tends to reduce the DC offset more accurately.

24. The radio-frequency receiver circuitry of claim 23, wherein the location of the at least one pole is adjustable by modifying a gain of the DC offset reduction circuitry.

25. The radio-frequency receiver circuitry of claim 24, wherein adjustment of the location of the at least one pole completes before a reception of a burst of data by the receiver analog circuitry begins.

26. The radio-frequency receiver circuitry of claim 25, used within a radio-frequency transceiver circuitry.

27. The radio-frequency receiver circuitry of claim 25, further comprising programmable gain amplifier circuitry coupled to the combiner circuitry and to the analog-to-digital circuitry, the programmable gain amplifier circuitry configured to apply a programmable gain to the difference signal to produce an amplified difference signal, the programmable gain amplifier circuitry further configured to provide the amplified difference signal to the analog-to-digital converter circuitry.

28. The radio-frequency receiver circuitry of claim 27, used within a radio-frequency transceiver circuitry.

29. A method of receiving a radio-frequency (RF) signal, comprising:

down-converting the radio-frequency signal within a receiver analog circuitry to generate a down-converted signal;

converting the down-converted signal to a digital output signal by using an analog-to-digital converter circuitry that resides within the receiver analog circuitry; and

feeding back to an input of the analog-to-digital converter circuitry a feedback signal that relates to the digital output signal,

wherein feeding back the feedback signal to an input of the analog-to-digital converter tends to reduce a DC offset of the receiver analog circuitry.

30. The method of claim 29, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises:

subtracting the feedback signal from the down-converted signal to generate a difference signal; and

supplying the difference signal to the input of the analog-to-digital converter circuitry.

31. The method of claim 30, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises:

filtering the digital output signal to generate a filtered digital signal; and

converting the filtered digital signal to the feedback signal by using a digital-to-analog converter circuitry.

32. The method of claim 31, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry comprises adjusting a location of at least one pole within the receiver analog circuitry.

[redacted]

33. The method of claim 32, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises adjusting at an initial point in time the location of the at least one pole so that the DC offset tends to be reduced quickly.

34. The method of claim 33, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises adjusting the location of the at least one pole at least once more after the initial point in time so that the DC offset tends to be reduced accurately.

35. The method of claim 34, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises adjusting the location of the at least one pole by modifying a gain within the receiver analog circuitry.

36. The method of claim 35, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises completing the adjustment of the location of the at least one pole before a reception of a burst of data by the receiver analog circuitry begins.

37. The method of claim 36, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises holding substantially constant the feedback signal before a reception of a burst of data begins.

38. The method of claim 37, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises:

applying a programmable gain to the difference signal to produce an amplified difference signal; and

supplying the amplified difference signal to the input of the analog-to-digital converter circuitry.

39. The method of claim 38, wherein converting the down-converted signal to a digital output signal comprises using a sigma-delta analog-to-digital converter circuitry that resides within the receiver analog circuitry.

40. The method of claim 39, further comprising supplying the digital output signal to a receiver digital circuitry.

41. The method of claim 40, further comprising processing the digital output signal in the receiver digital circuitry to generate a baseband signal.

42. The method of claim 41, further comprising providing the baseband signal to a baseband processor circuitry.

43. The method of claim 42, wherein receiving the radio-frequency signal further comprises receiving the radio-frequency signal within a low intermediate-frequency radio-frequency receiver circuitry.

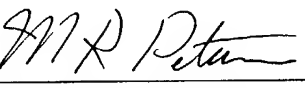
44. The method of claim 43, wherein receiving the radio-frequency signal further comprises receiving the radio-frequency signal within a radio-frequency transceiver circuitry.

CONCLUSION

With this amendment, claims 1 and 3-44 are pending. Claim 2 has been cancelled. A check in the amount of $414.00 is enclosed for the addition of 23 dependent claims.

Should any fees under 37 CFR 1.16-1.21 be required for any reason relating to the enclosed materials, the Commissioner is authorized to deduct such fees from Deposit Account No. 10-1205/SILA:098. The examiner is invited to contact the undersigned at the phone number indicated below with any questions or comments, or to otherwise facilitate expeditious and compact prosecution of the application.

Respectfully submitted,



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APPENDIX

MARKED UP VERSION OF AMENDMENTS

AS REQUIRED BY RULE 121

In The Specification:

Please replace the paragraph beginning on page 1, line 27 and ending on page 2, line 2 with the following:

--Furthermore, this patent application incorporates by reference the following patent documents: U.S. Patent Application Serial No. [_____] 10/075,122, Attorney Docket No. SILA:078, titled "Digital Architecture for Radio-Frequency Apparatus and Associated Methods"; and U.S. Patent Application Serial No. [_____] 10/075,099, Attorney Docket No. SILA:097, titled "Notch Filter for DC Offset Reduction in Radio-Frequency Apparatus and Associated Methods."--

In The Claims:

[2. A radio-frequency (RF) apparatus, comprising:

a first circuit partition, comprising receiver analog circuitry configured to produce a digital receive signal from an analog radio-frequency signal; and

a second circuit partition, comprising receiver digital circuitry configured to accept the digital receive signal, wherein the first and second circuit partitions are partitioned so that interference effects between the first circuit partition and the second circuit partition tend to be reduced.]

--3. (New) The radio-frequency receiver circuitry of claim 1, further comprising:

a combiner circuitry configured to provide to the analog-to-digital circuitry an in-phase difference signal and a quadrature difference signal,

wherein the combiner circuitry subtracts an in-phase output signal of the DC offset reduction circuitry from the in-phase down-converted signal to produce the in-phase difference signal, and

wherein the combiner circuitry subtracts a quadrature output signal of the DC offset reduction circuitry from the quadrature down-converted signal to produce the quadrature difference signal.--

--4. (New) The radio-frequency receiver circuitry of claim 3, wherein the DC offset reduction circuitry further comprises a digital-to-analog circuitry configured to provide the in-phase and quadrature output signals of the DC offset reduction circuitry.--

--5. (New) The radio-frequency receiver circuitry of claim 4, wherein the DC offset reduction circuitry further comprises a filter circuitry configured to process the in-phase and quadrature digital output signals to provide an in-phase filtered digital output signal and a quadrature filtered digital output signal, the filter circuitry further configured to provide the in-phase and quadrature filtered digital output signals to the digital-to-analog circuitry.--

--6. (New) The radio-frequency receiver circuitry of claim 5, wherein a transfer function of the DC offset reduction circuitry has at least one pole the location of which is adjustable over an adjustment cycle of the DC offset reduction circuitry.--

--7. (New) The radio-frequency receiver circuitry of claim 6, wherein the location of the at least one pole is adjusted in an initial part of the adjustment cycle of the DC offset reduction circuitry so that the DC offset reduction circuitry tends to settle quickly.--

--8. (New) The radio-frequency receiver circuitry of claim 7, wherein the location of the at least one pole is further adjusted in a later part of the adjustment cycle of the DC offset reduction circuitry so that the DC offset reduction circuitry tends to remove the DC offset more accurately.--

--9. (New) The radio-frequency receiver circuitry of claim 8, wherein the location of the at least one pole is adjusted by modifying a gain of the DC offset reduction circuitry.--

--10. (New) The radio-frequency receiver circuitry of claim 9, wherein the location of the at least one pole is adjusted before a reception of a burst of data begins.--

--11. (New) The radio-frequency receiver circuitry of claim 10, wherein the in-phase and quadrature output signals of the DC offset reduction circuitry become substantially constant before the reception of the burst of data begins.--

--12. (New) The radio-frequency receiver circuitry of claim 11, wherein the filter circuitry comprises a digital filter circuitry.--

--13. (New) The radio-frequency receiver circuitry of claim 12, wherein the digital filter circuitry comprises a low-pass filter circuitry.--

--14. (New) The radio-frequency receiver circuitry of claim 13, wherein the low-pass filter circuitry comprises an integrator circuitry.--

--15. (New) The radio-frequency receiver circuitry of claim 14, wherein the analog-to-digital converter circuitry comprises a sigma-delta analog-to-digital converter circuitry.--

--16. (New) The radio-frequency receiver circuitry of claim 15 used in a radio-frequency transceiver circuitry.--

--17. (New) The radio-frequency receiver circuitry of claim 15 used in a low intermediate-frequency (IF) radio-frequency receiver circuitry.--

--18. (New) A radio-frequency (RF) receiver circuitry, comprising:

receiver analog circuitry included within a first integrated circuit, the receiver analog circuitry, comprising:

down-converter circuitry configured to receive and down-convert a radio-frequency input signal to generate a down-converted signal;

an analog-to-digital converter circuitry to convert the down-converted signal to a digital output signal; and

DC offset reduction circuitry coupled to the analog-to-digital converter circuitry, wherein the DC offset reduction circuitry tends to reduce a DC offset of the receiver analog circuitry; and

receiver digital circuitry included within a second integrated circuit, the receiver digital circuitry configured to receive and process the digital output signal to generate a processed digital signal.--

--19. (New) The radio-frequency receiver circuitry of claim 18, further comprising a combiner circuitry configured to provide a difference signal to the analog-to-digital circuitry, wherein the combiner circuitry subtracts an output signal of the DC offset reduction circuitry from the down-converted signal to produce the difference signal.--

--20. (New) The radio-frequency receiver circuitry of claim 19, wherein the DC offset reduction circuitry further comprises a feedback loop that includes a cascade coupling of a filter circuitry and a digital-to-analog circuitry, wherein the filter circuitry receives the

digital output signal, and wherein the digital-to-analog circuitry provides the output signal of the DC offset reduction circuitry.--

--21. (New) The radio-frequency receiver circuitry of claim 20, wherein a transfer function of the DC offset reduction circuitry has at least one pole the location of which is adjustable so as to modify the settling time of the DC offset reduction circuitry.--

--22. (New) The radio-frequency receiver circuitry of claim 21, wherein the location of the at least one pole is adjusted at an initial point in time so that the DC offset reduction circuitry tends to settle quickly.--

--23. (New) The radio-frequency receiver circuitry of claim 22, wherein the location of the at least one pole is adjusted at least once more after the initial point in time so that the DC offset reduction circuitry tends to reduce the DC offset more accurately.--

--24. (New) The radio-frequency receiver circuitry of claim 23, wherein the location of the at least one pole is adjustable by modifying a gain of the DC offset reduction circuitry.--

--25. (New) The radio-frequency receiver circuitry of claim 24, wherein adjustment of the location of the at least one pole completes before a reception of a burst of data by the receiver analog circuitry begins.--

--26. (New) The radio-frequency receiver circuitry of claim 25, used within a radio-frequency transceiver circuitry.--

--27. (New) The radio-frequency receiver circuitry of claim 25, further comprising programmable gain amplifier circuitry coupled to the combiner circuitry and to the

analog-to-digital circuitry, the programmable gain amplifier circuitry configured to apply a programmable gain to the difference signal to produce an amplified difference signal, the programmable gain amplifier circuitry further configured to provide the amplified difference signal to the analog-to-digital converter circuitry.--

--28. (New) The radio-frequency receiver circuitry of claim 27, used within a radio-frequency transceiver circuitry.--

--29. (New) A method of receiving a radio-frequency (RF) signal, comprising:

down-converting the radio-frequency signal within a receiver analog circuitry to generate a down-converted signal;

converting the down-converted signal to a digital output signal by using an analog-to-digital converter circuitry that resides within the receiver analog circuitry; and

feeding back to an input of the analog-to-digital converter circuitry a feedback signal that relates to the digital output signal,

wherein feeding back the feedback signal to an input of the analog-to-digital converter tends to reduce a DC offset of the receiver analog circuitry.--

--30. (New) The method of claim 29, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises:

subtracting the feedback signal from the down-converted signal to generate a difference signal; and

supplying the difference signal to the input of the analog-to-digital converter circuitry.--

--31. (New) The method of claim 30, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises:

filtering the digital output signal to generate a filtered digital signal; and

converting the filtered digital signal to the feedback signal by using a digital-to-analog converter circuitry.--

--32. (New) The method of claim 31, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry comprises adjusting a location of at least one pole within the receiver analog circuitry.--

--33. (New) The method of claim 32, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises adjusting at an initial point in time the location of the at least one pole so that the DC offset tends to be reduced quickly.--

--34. (New) The method of claim 33, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises adjusting the location of the at least one pole at least once more after the initial point in time so that the DC offset tends to be reduced accurately.--

--35. (New) The method of claim 34, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises adjusting the location of the at least one pole by modifying a gain within the receiver analog circuitry.--

--36. (New) The method of claim 35, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises completing the adjustment of the location of the at least one pole before a reception of a burst of data by the receiver analog circuitry begins.--

--37. (New) The method of claim 36, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises holding substantially constant the feedback signal before a reception of a burst of data begins.--

--38. (New) The method of claim 37, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises:

applying a programmable gain to the difference signal to produce an amplified difference signal; and

supplying the amplified difference signal to the input of the analog-to-digital converter circuitry.--

--39. (New) The method of claim 38, wherein converting the down-converted signal to a digital output signal comprises using a sigma-delta analog-to-digital converter circuitry that resides within the receiver analog circuitry.--

--40. (New) The method of claim 39, further comprising supplying the digital output signal to a receiver digital circuitry.--

--41. (New) The method of claim 40, further comprising processing the digital output signal in the receiver digital circuitry to generate a baseband signal.--

--42. (New) The method of claim 41, further comprising providing the baseband signal to a baseband processor circuitry.--

--43. (New) The method of claim 42, wherein receiving the radio-frequency signal further comprises receiving the radio-frequency signal within a low intermediate-frequency radio-frequency receiver circuitry.--

--44. (New) The method of claim 43, wherein receiving the radio-frequency signal further comprises receiving the radio-frequency signal within a radio-frequency transceiver circuitry.--